IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) A device comprising:

a plurality of data lines for transferring both data and auxiliary information, wherein at least one of the data lines is configured for serially transferring at least one bit of the data with at least one bit of the auxiliary information;

a memory array for storing the data;

an auxiliary circuit having auxiliary lines for carrying auxiliary information; and

a transceiver circuit connected to the memory array and the data lines for transferring the data between the memory array and the data lines, the transceiver circuit also connects to the auxiliary circuit for transferring the auxiliary information between the auxiliary lines and the data lines.

2. (Original) The device of claim 1, wherein the auxiliary circuit includes an inversion controller connected to the transceiver circuit and the memory array for conditionally inverting the data.

3. (Original) The device of claim 2, wherein the auxiliary circuit further includes a parity controller connected to the transceiver circuit and the memory array for generating a number of parity codes for the data.

4. (Original) The device of claim 3, wherein the auxiliary circuit further includes a temperature reporting circuit connected to the transceiver circuit for generating temperature information of the device.

5. (Original) The device of claim 4, wherein the auxiliary circuit further includes a calibrating circuit connected to the transceiver circuit for providing a time delay based on the auxiliary information.

6. (Previously Presented) A device comprising:

a plurality of data lines for transferring both data and auxiliary information, wherein at least one of the data lines is configured for serially transferring at least one bit of the data with at least one bit of the auxiliary information;

a memory array for storing data;

an auxiliary circuit including a parity controller connected to the memory array for generating a plurality of parity codes for the data; and

a transceiver circuit connected to the memory array and the data lines for transferring the data between the memory array and the data lines, the transceiver circuit also connects to the parity controller for transferring the parity codes between the parity controller and the data lines.

7. (Original) The device of claim 6, wherein the parity controller includes a number of comparators for comparing bits of the data.

8. (Original) The device of claim 7, wherein the parity controller includes a storage unit for storing the parity codes.

9. (Original) The device of claim 6, wherein the auxiliary circuit further includes an inversion controller connected to the transceiver circuit and the memory array for conditionally inverting the data transferred between the transceiver circuit and the memory array.

10. (Currently Amended) A device comprising:

a plurality of data lines;

a memory array for storing data;

an auxiliary circuit including a parity controller connected to the memory array for generating a plurality of parity codes for the data; and

a transceiver circuit connected to the memory array and the data lines for transferring the data between the memory array and the data lines, the transceiver circuit also connects to the parity controller for transferring the parity codes between the parity controller and the data lines, wherein the auxiliary circuit further includes an inversion controller connected to the transceiver

circuit and the memory array for conditionally inverting the data transferred between the transceiver circuit and the memory array, wherein the inversion controller includes a storage unit for storing inverting codes of the data, and wherein the transceiver circuit connects to the storage unit for transferring the inverting codes between the ~~inverting parity~~ inversion controller and the data lines.

11. (Previously Presented) A device comprising:

a plurality of data lines for transferring both data and auxiliary information, wherein at least one of the data lines is configured for serially transferring at least one bit of the data with at least one bit of the auxiliary information;

a memory array for storing input data and output data;

an input auxiliary circuit configured for receiving input auxiliary information of the input data and configured for performing a function on the input data;

an output auxiliary circuit configured for generating output auxiliary information of the output data and configured for performing a function on the output data; and

a transceiver circuit connected to the memory array and the data lines for transferring the input and output data between the memory array and the data lines, the transceiver circuit also connects to the input and output auxiliary circuits for transferring the input and output auxiliary information between the input and output auxiliary circuits and the data lines.

12. (Original) The device of claim 11, wherein the output auxiliary circuit includes an output inverting circuit for conditionally inverting the output data based on the output auxiliary information.

13. (Original) The device of claim 12, wherein the output auxiliary circuit further includes an output parity generator for generating a number of parity codes for the output data.

14. (Original) The device of claim 13, wherein the output auxiliary circuit further includes a temperature reporting circuit for generating temperature information of the device.

15. (Original) The device of claim 14, wherein the input auxiliary circuit includes an input inverting circuit for conditionally inverting the input data based on the input auxiliary information.

16. (Original) The device of claim 15, wherein the input auxiliary circuit further includes an input parity generator for generating a number of parity codes for the input data.

17. (Original) The device of claim 16, wherein the input auxiliary circuit further includes a calibrating circuit for providing a time delay based on the input auxiliary information.

18.-55. (Canceled)

56. (Currently Amended) A device comprising:

a plurality of data lines for transferring both data and auxiliary information;

a memory array for storing the data;

an auxiliary circuit having auxiliary lines for carrying auxiliary information, the auxiliary circuit including an inversion controller for conditionally inverting the data, wherein the inversion controller includes a storage unit for storing inverting codes of the data; and

a transceiver circuit connected to the memory array and the data lines for transferring the data between the memory array and the data lines, the transceiver circuit also connects to the auxiliary circuit for transferring the auxiliary information between the auxiliary lines and the data lines.

57. (Previously Presented) The device of claim 56, wherein the auxiliary circuit further includes a parity controller connected to the transceiver circuit and the memory array for generating a number of parity codes for the data.

58. (Previously Presented) The device of claim 56, wherein the auxiliary circuit further includes a temperature reporting circuit connected to the transceiver circuit for generating temperature information of the device.

59. (Previously Presented) The device of claim 56, wherein the auxiliary circuit further includes a calibrating circuit connected to the transceiver circuit for providing a time delay based on the auxiliary information.

60. (Currently Amended) A device comprising:

a plurality of data lines for transferring both data and auxiliary information;

a memory array for storing data;

an auxiliary circuit including a parity controller connected to the memory array for generating a plurality of parity codes for the data, and inversion controller connected to the memory array for conditionally inverting the data, wherein the inversion controller includes a storage unit for storing inverting codes of the data; and

a transceiver circuit connected to the memory array and the data lines for transferring the data between the memory array and the data lines, the transceiver circuit also connects to the parity controller for transferring the parity codes between the parity controller and the data lines.

61. (Previously Presented) The device of claim 60, wherein the parity controller includes a number of comparators for comparing bits of the data.

62. (Previously Presented) The device of claim 60, wherein the parity controller includes a storage unit for storing the parity codes.

63. (Previously Presented) A device comprising:

a plurality of data lines for transferring both data and auxiliary information;

a memory array for storing input data and output data;

an input auxiliary circuit configured for receiving input auxiliary information of the input data and configured for performing a function on the input data;

an output auxiliary circuit configured for generating output auxiliary information of the output data and configured for conditionally inverting the output data based on the output auxiliary information; and

a transceiver circuit connected to the memory array and the data lines for transferring the input and output data between the memory array and the data lines, the transceiver circuit also connects to the input and output auxiliary circuits for transferring the input and output auxiliary information between the input and output auxiliary circuits and the data lines.

64. (Previously Presented) The device of claim 63, wherein the output auxiliary circuit includes an output parity generator for generating a number of parity codes for the output data.

65. (Previously Presented) The device of claim 63, wherein the output auxiliary circuit further includes a temperature reporting circuit for generating temperature information of the device.

66. (Previously Presented) The device of claim 63, wherein the input auxiliary circuit includes an input inverting circuit for conditionally inverting the input data based on the input auxiliary information.

67. (Previously Presented) The device of claim 63, wherein the input auxiliary circuit further includes an input parity generator for generating a number of parity codes for the input data.

68. (Previously Presented) The device of claim 63, wherein the input auxiliary circuit further includes a calibrating circuit for providing a time delay based on the input auxiliary information.